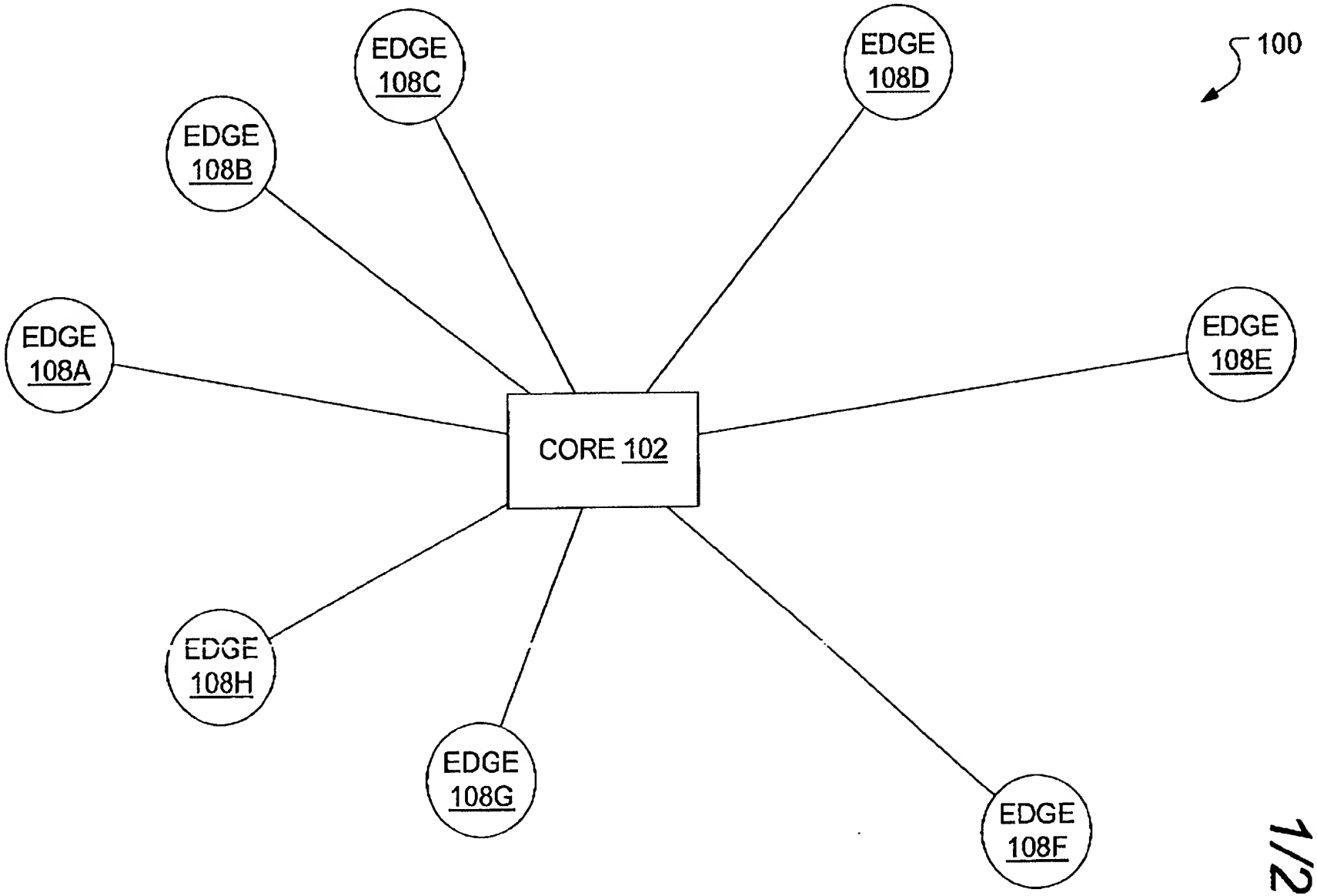


FIG. 1

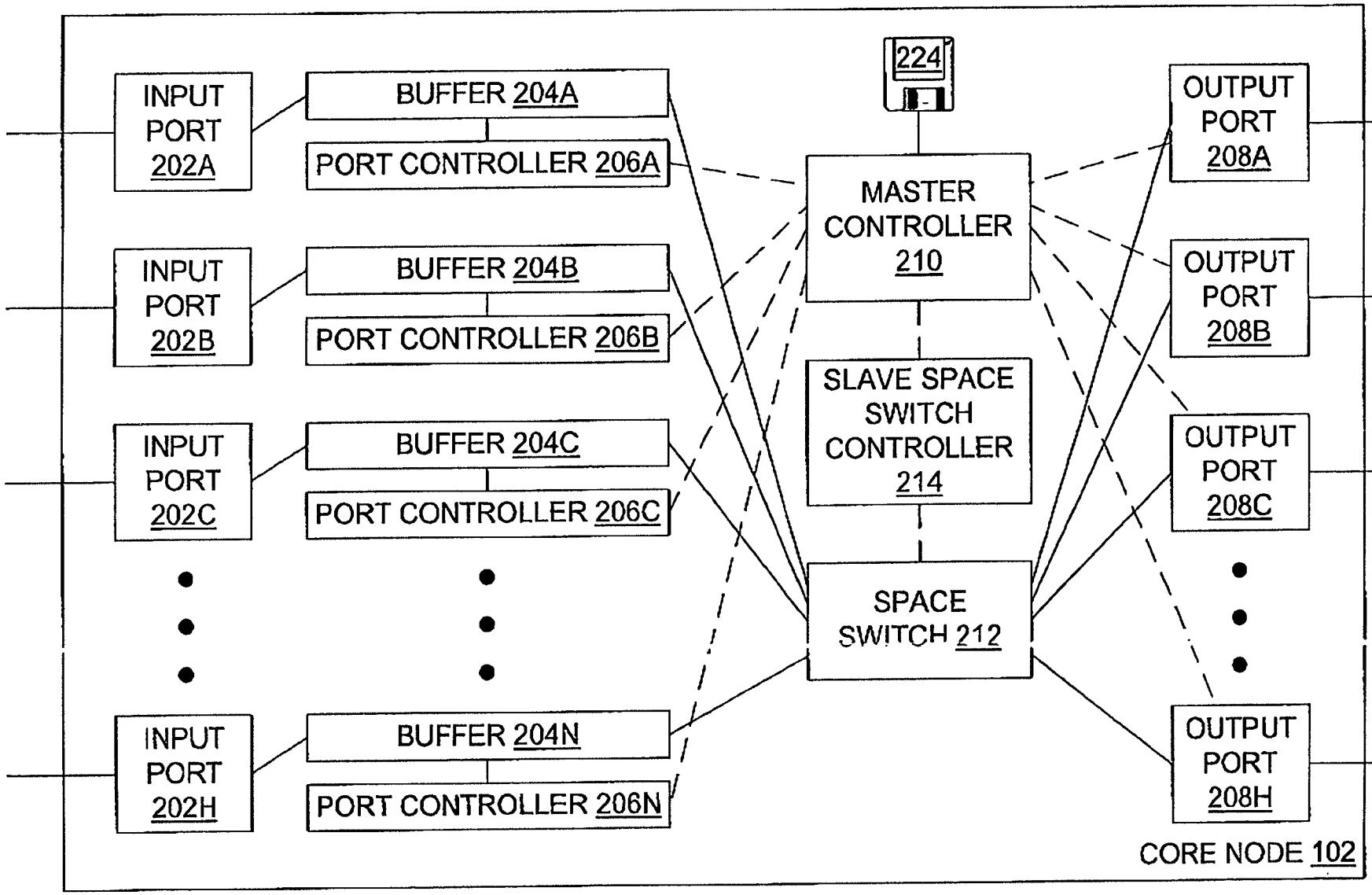


FIG. 2

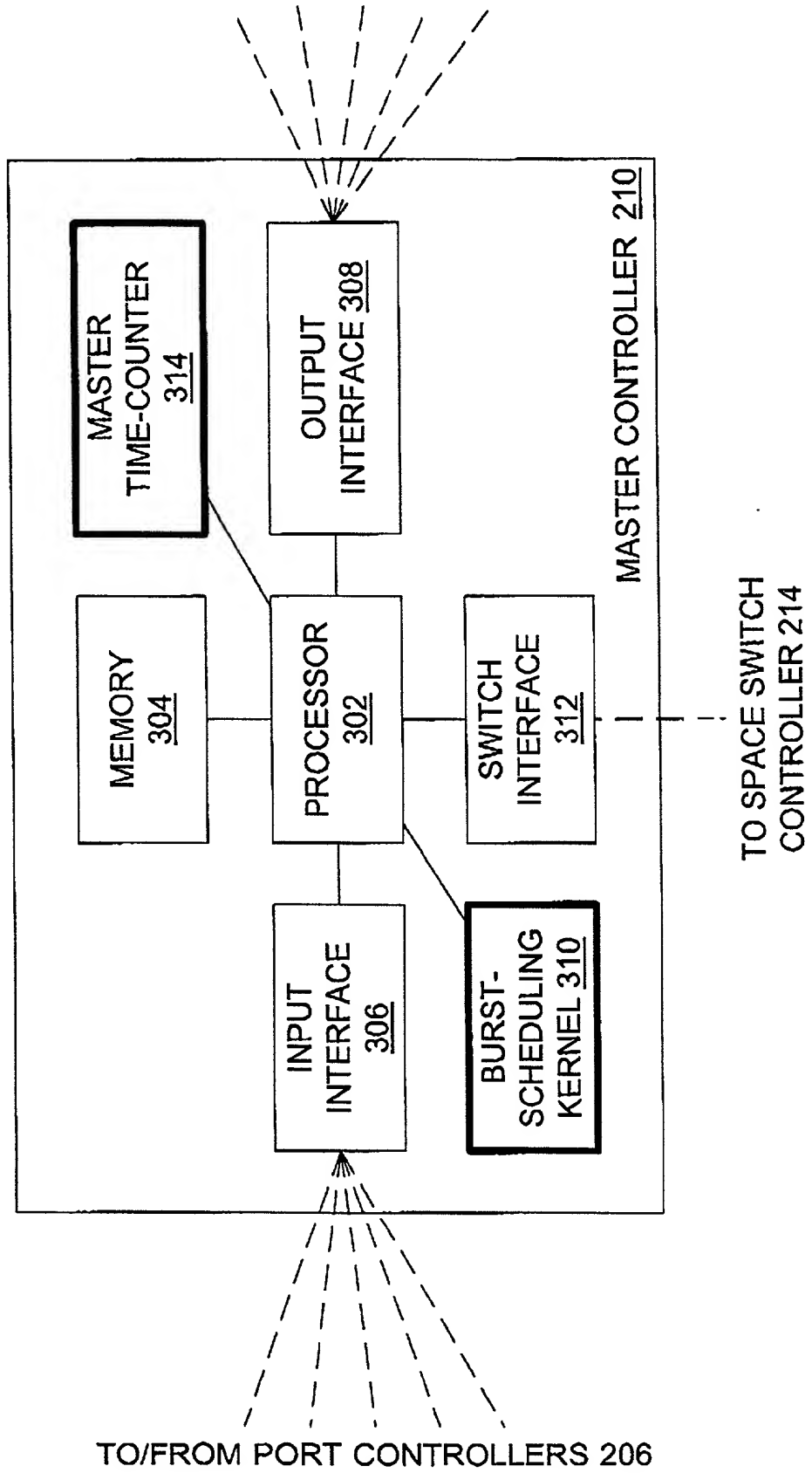
FROM OUTPUT PORTS 208
MASTER CONTROLLER 210
MASTER TIME-COUNTER 314
OUTPUT INTERFACE 308
MEMORY 304
PROCESSOR 302
SWITCH INTERFACE 312
INPUT INTERFACE 306
BURST-SCHEDULING KERNEL 310
TO SPACE SWITCH CONTROLLER 214
TO/FROM PORT CONTROLLERS 206

FIG. 3

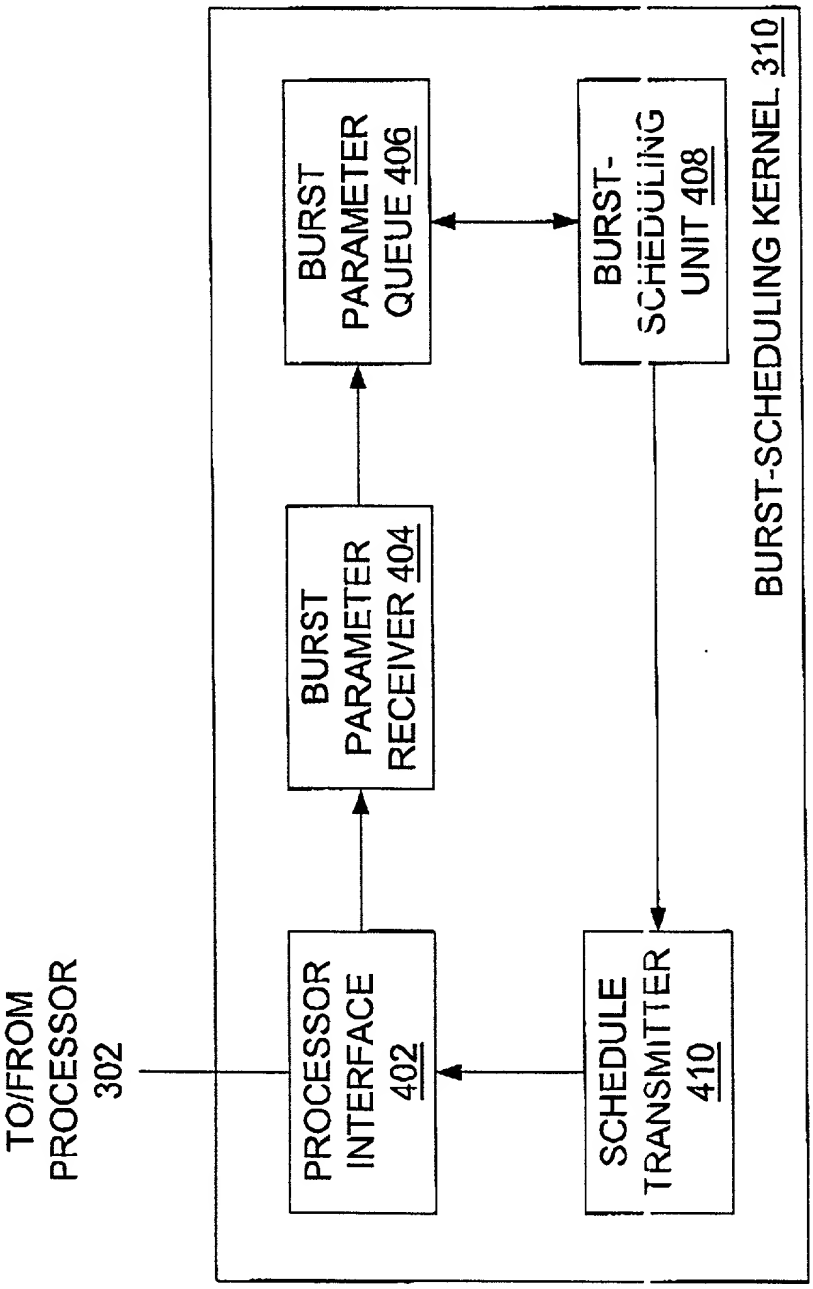
TO/FROM PROCESSOR 302
PROCESSOR INTERFACE 402
BURST PARAMETER RECEIVER 404
BURST PARAMETER QUEUE 406
BURST-SCHEDULE UNIT 408
SCHEDULE TRANSMITTER 410
BURST-SCHEDULING KERNEL 310

FIG. 4

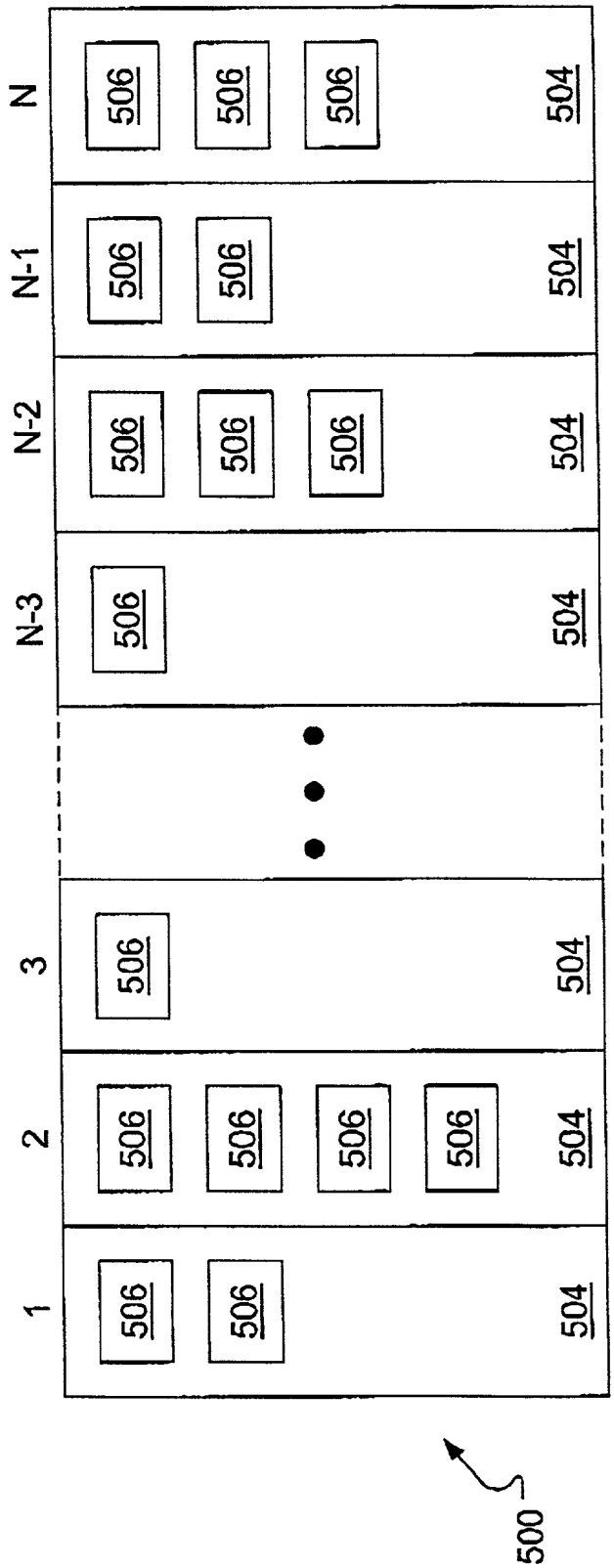


FIG. 5A

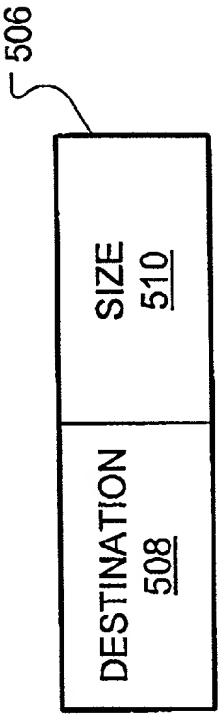


FIG. 5B

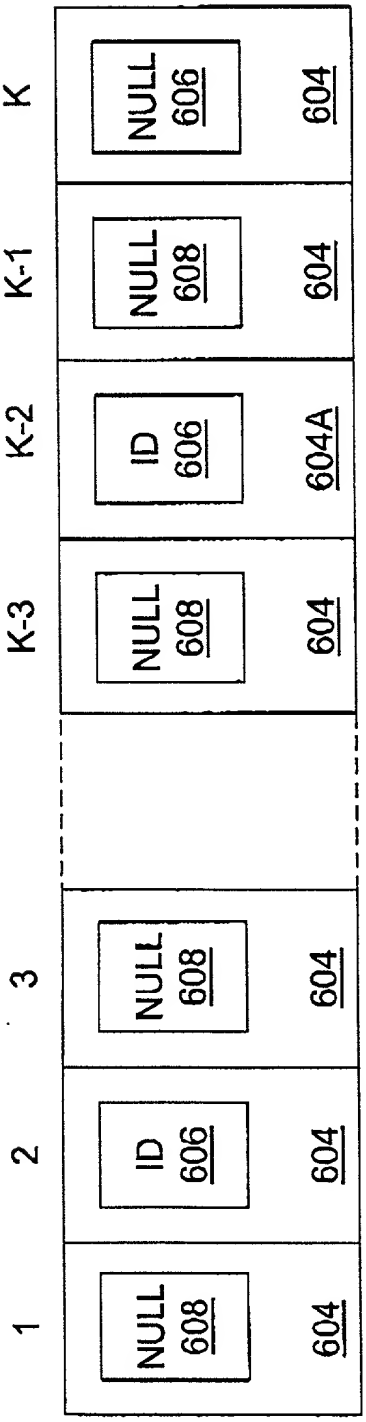
1
2
3
K-3
K-2
K-1
K
NULL 608
ID 606
NULL 608
NULL 608
ID 606
NULL 608
NULL 606
604
604
604
604
604A
604
604
600

FIG. 6

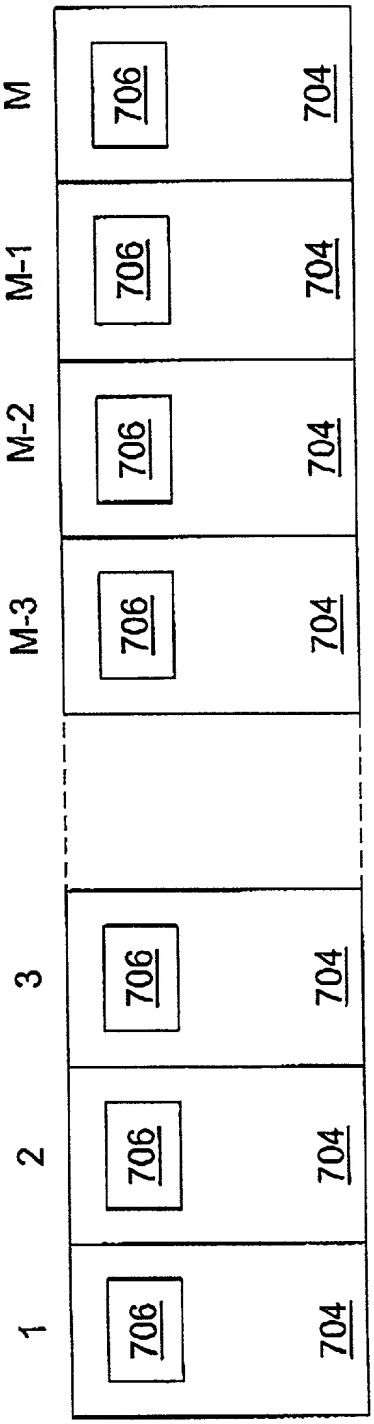


FIG. 7

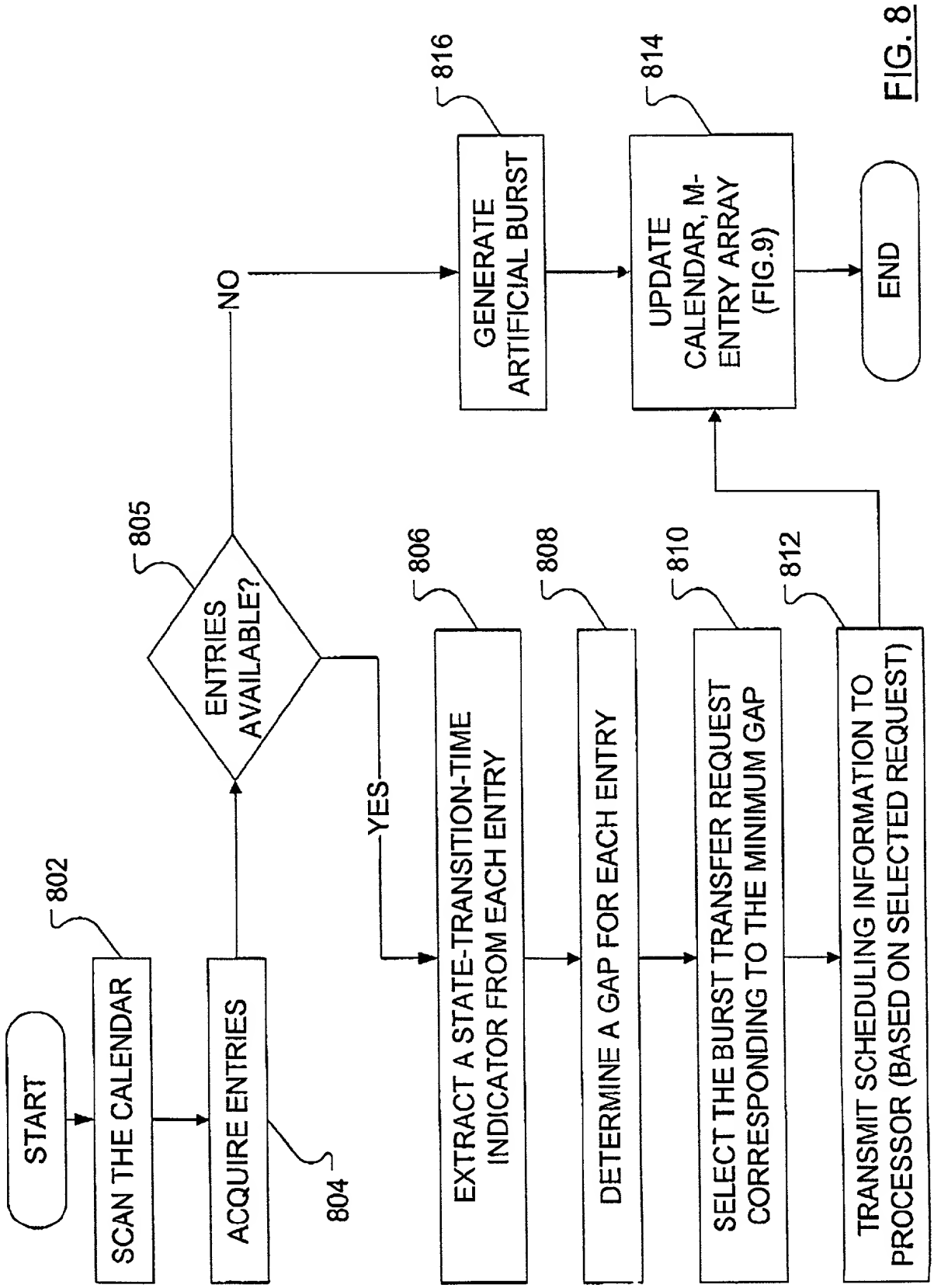
START
SCAN THE CALENDAR
802
ACQUIRE ENTRIES
804
ENTRIES AVAILABLE?
805
NO
YES
GENERATE ARTIFICIAL BURST
816
EXTRACT A STATE-TRANSITION-TIME INDICATOR FROM EACH ENTRY
806
DETERMINE A GAP FOR EACH ENTRY
808
SELECT THE BURST TRANSFER REQUEST CORRESPONDING TO THE MINIMUM GAP
810
TRANSMIT SCHEDULING INFORMATION TO PROCESSOR (BASED ON SELECTED REQUEST)
812
UPDATE CALENDAR, M-ENTRY ARRAY (FIG.9)
814
END

FIG. 8

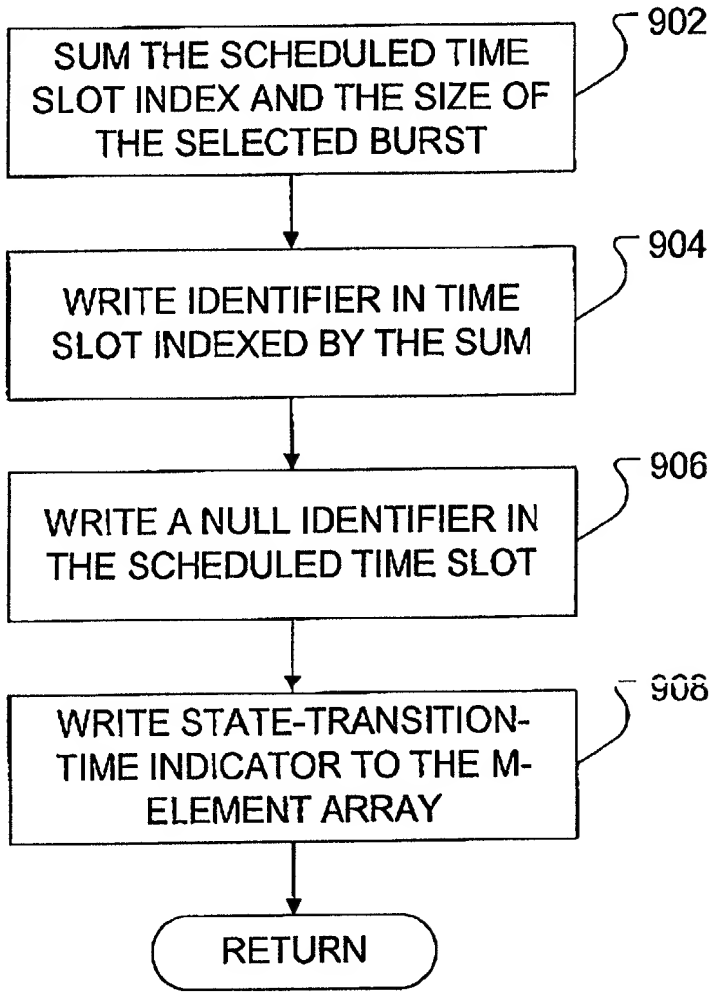


FIG. 9

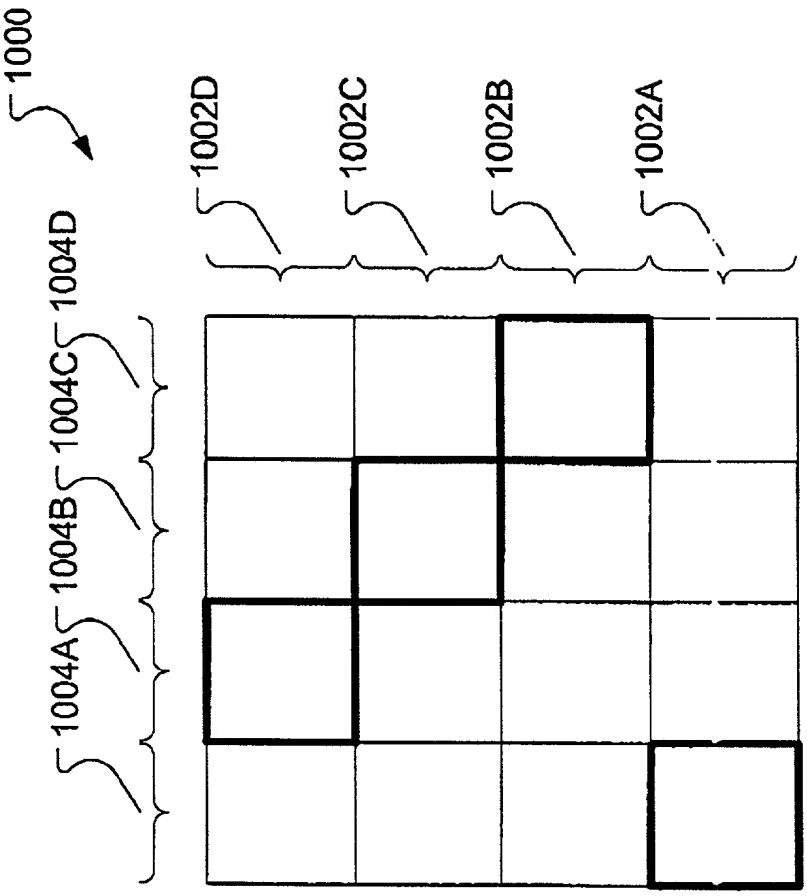


FIG. 10

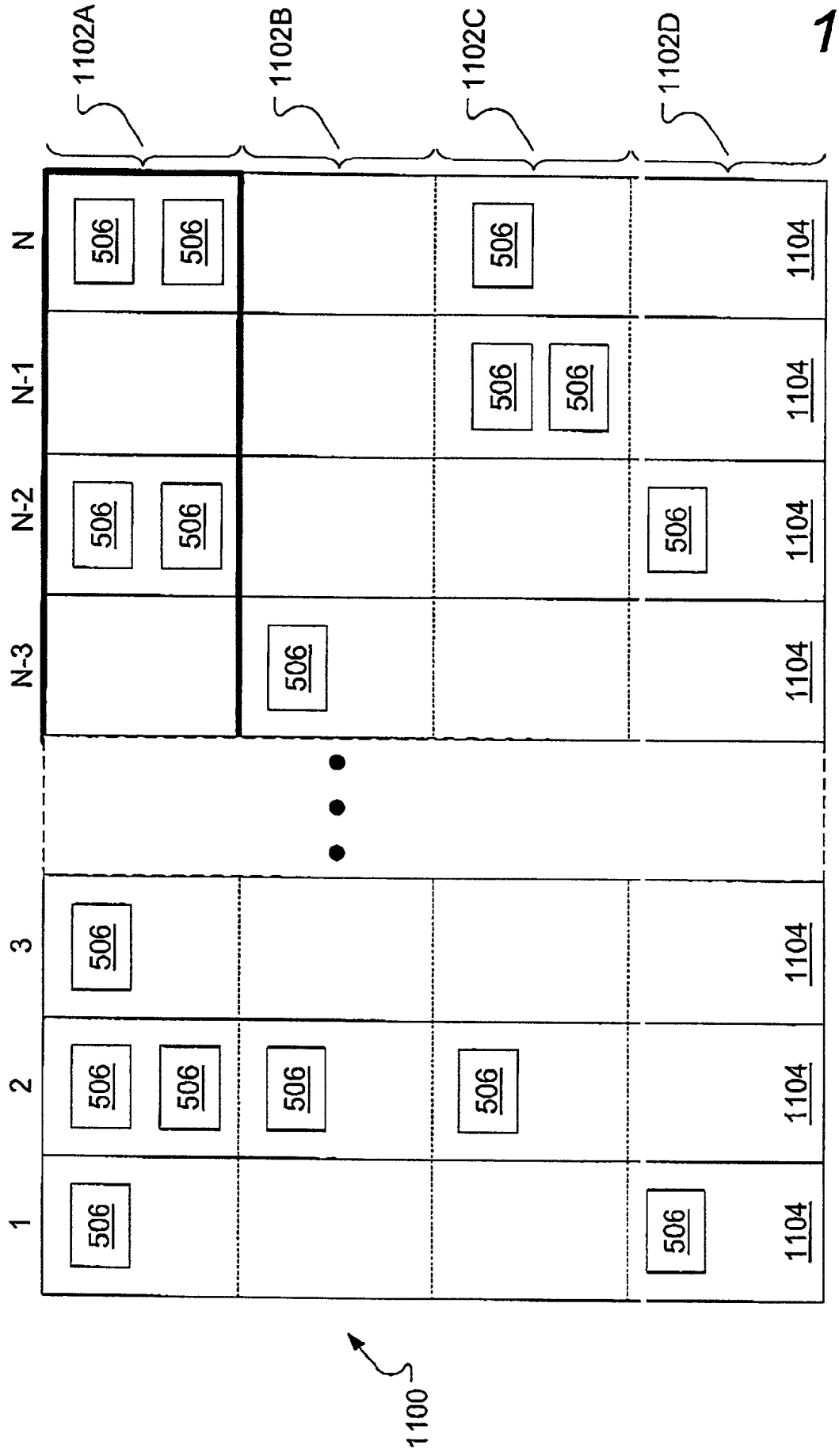


FIG. 11

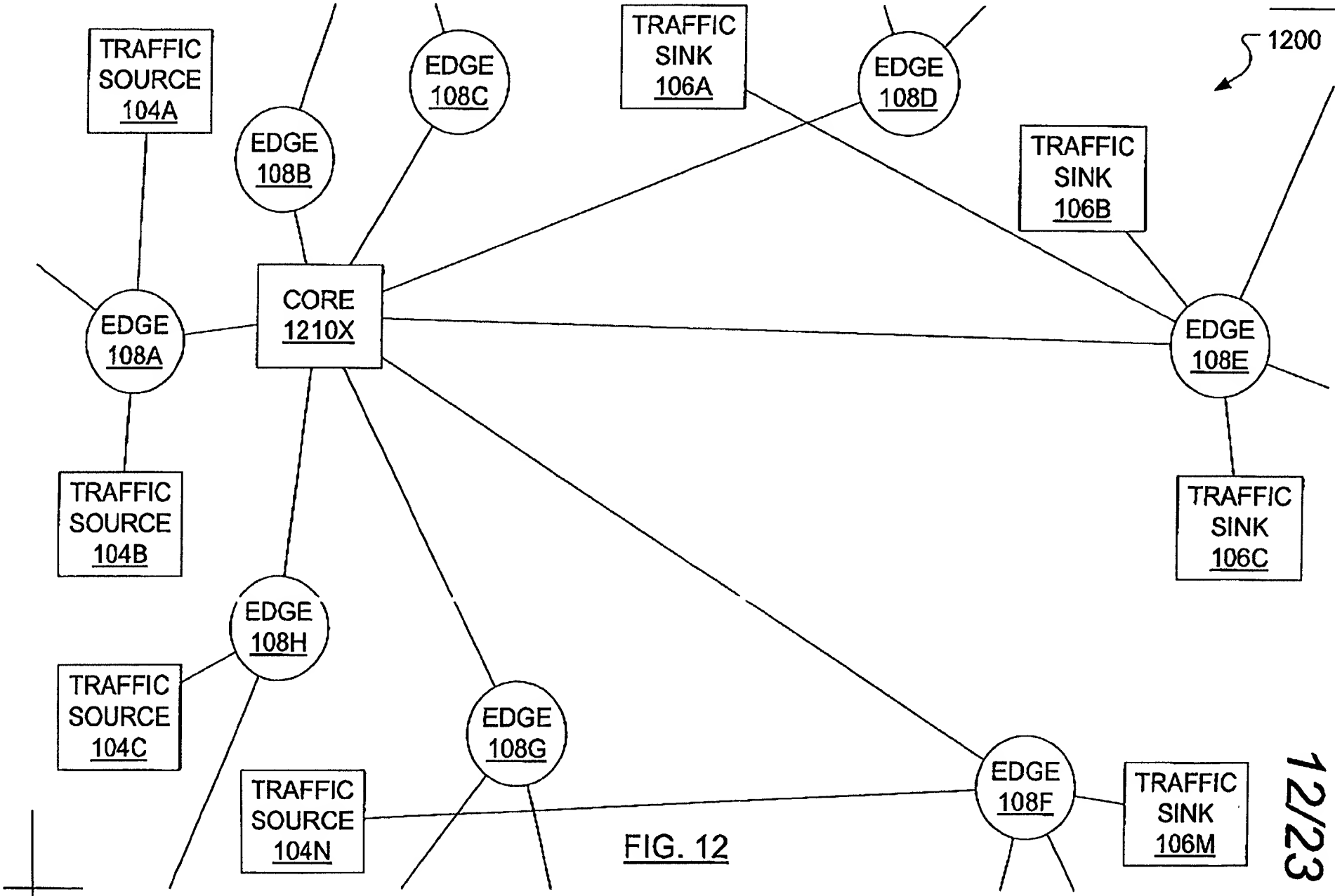


FIG. 12

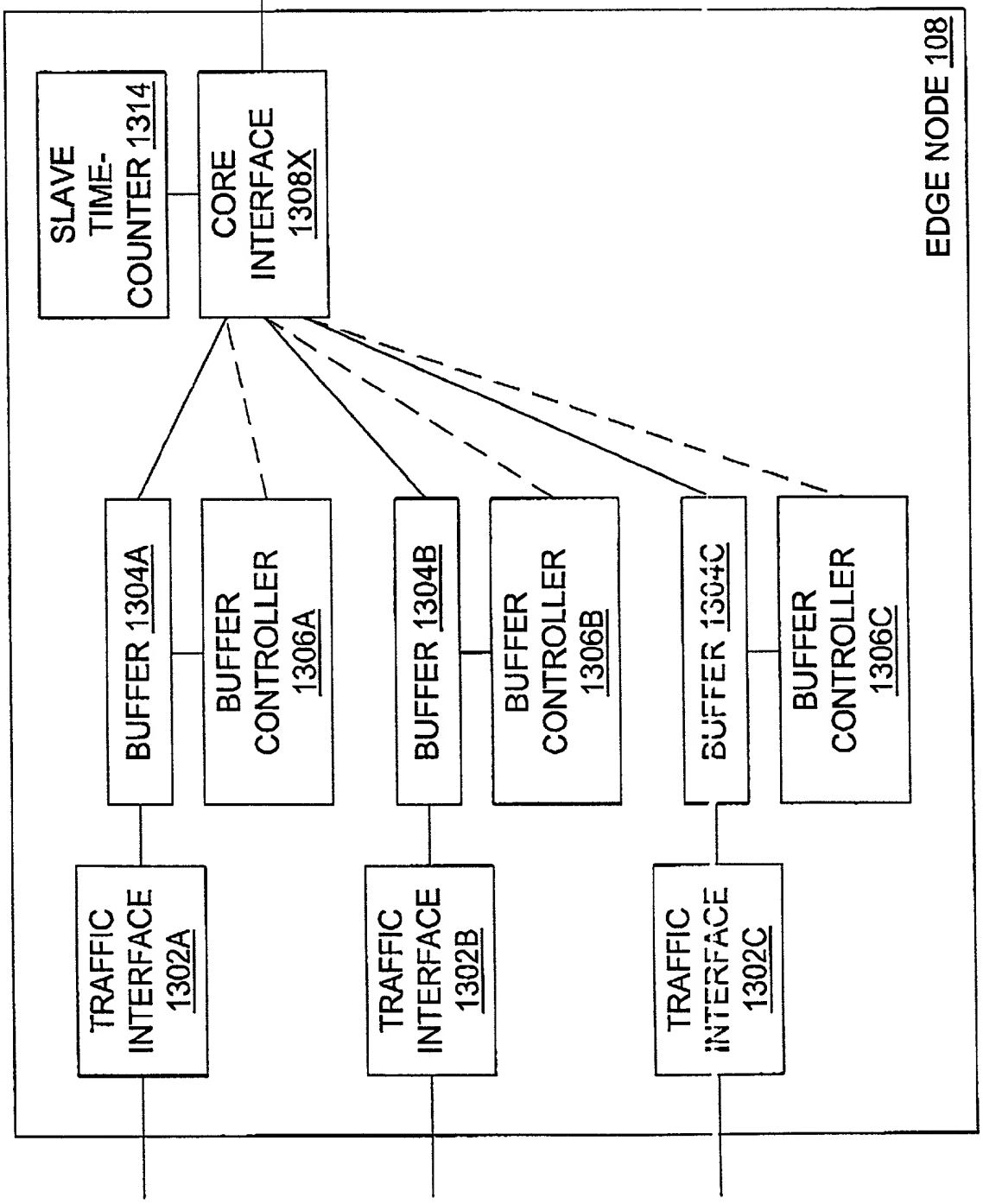
TO/FROM CORE NODE 1210X
SLAVE TIME-COUNTER 1314
CORE INTERFACE 1308X
EDGE NODE 108
BUFFER 1304A
BUFFER CONTROLLER 1306A
BUFFER 1304B
BUFFER CONTROLLER 1306B
BUFFER 1304C
BUFFER CONTROLLER 1306C
TRAFFIC INTERFACE 1302A
TRAFFIC INTERFACE 1302B
TRAFFIC INTERFACE 1302C

FIG. 13

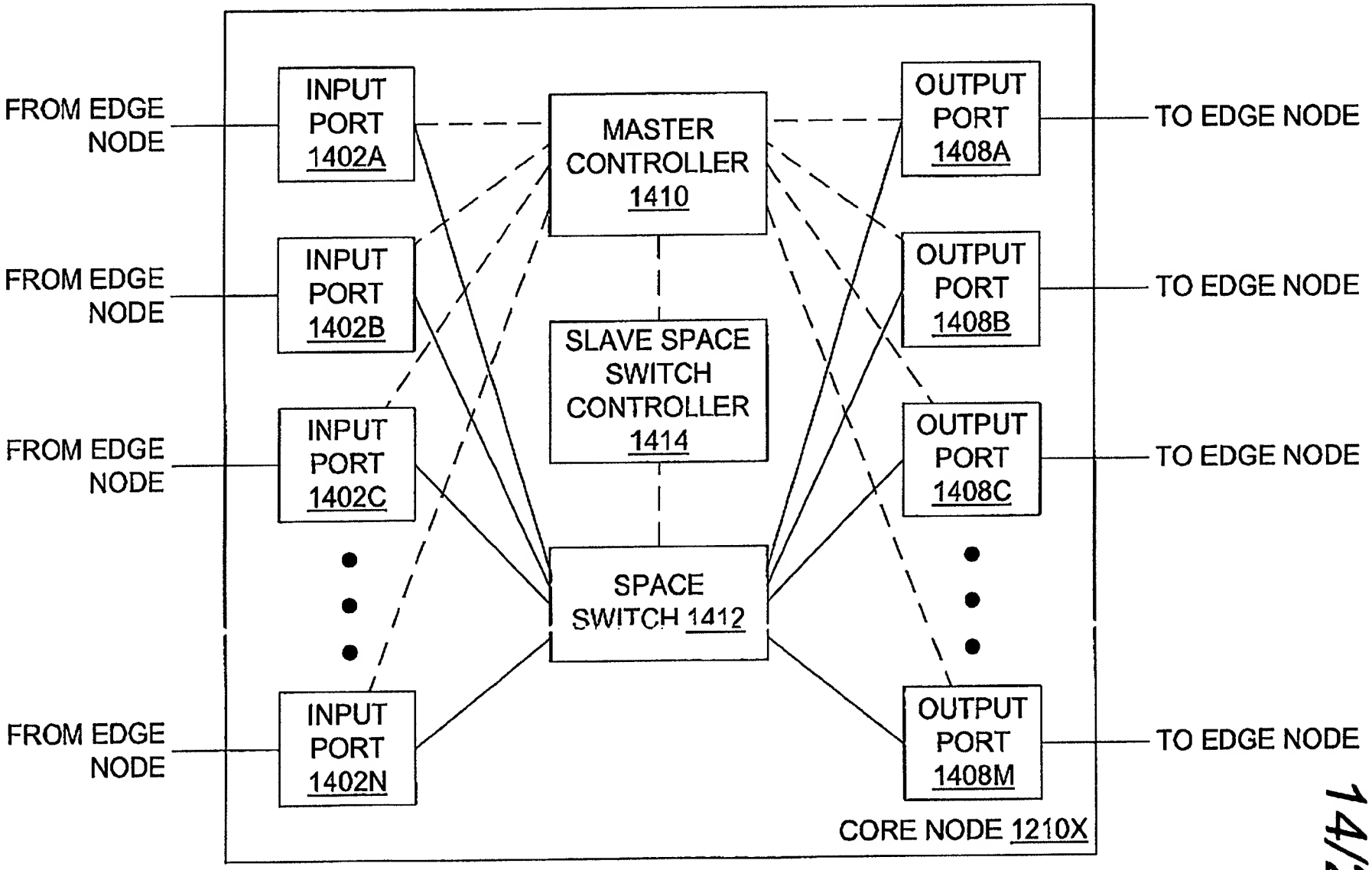


FIG. 14

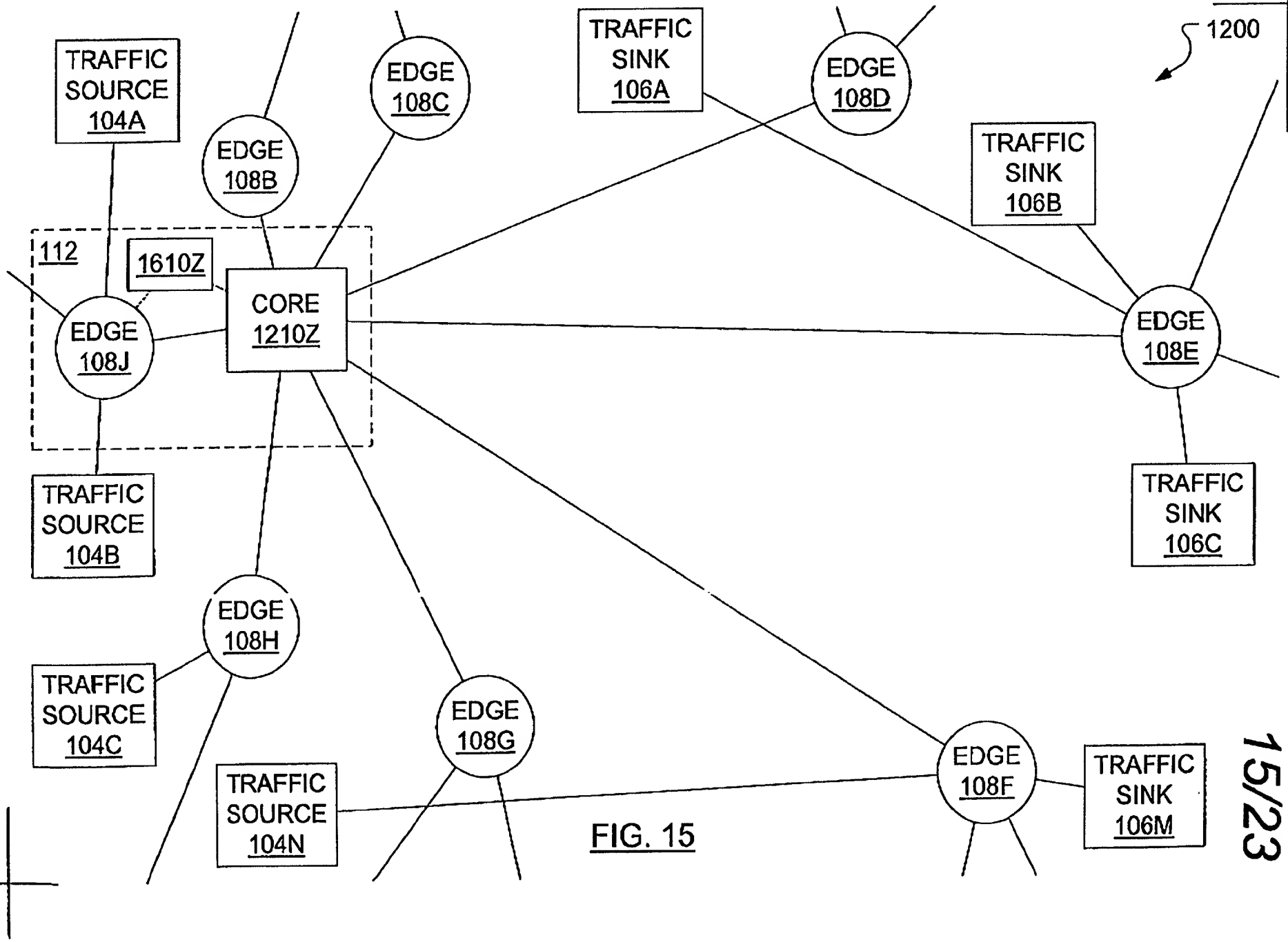


FIG. 15

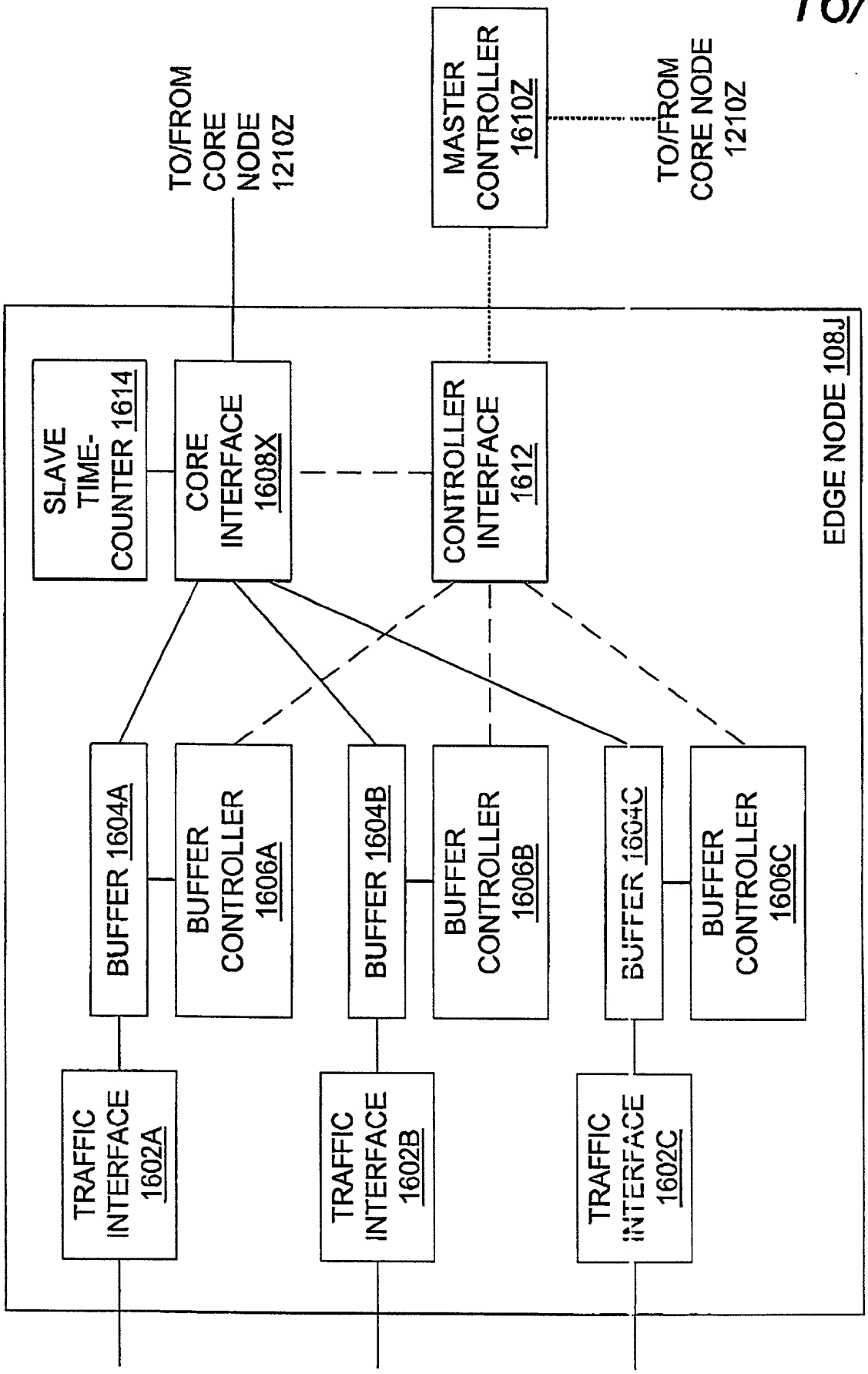
TO/FROM CORE NODE 1210Z
MASTER CONTROLLER 1610Z
TO/FROM CORE NODE 1210Z
SLAVE TIME-COUNTER 1614
CORE INTERFACE 1608X
CONTROLLER INTERFACE 1612
EDGE NODE 108J
BUFFER 1604A
BUFFER CONTROLLER 1606A
BUFFER 1604B
BUFFER CONTROLLER 1606B
BUFFER 1604C
BUFFER CONTROLLER 1606C
TRAFFIC INTERFACE 1602A
TRAFFIC INTERFACE 1602B
TRAFFIC INTERFACE 1602C

FIG. 16

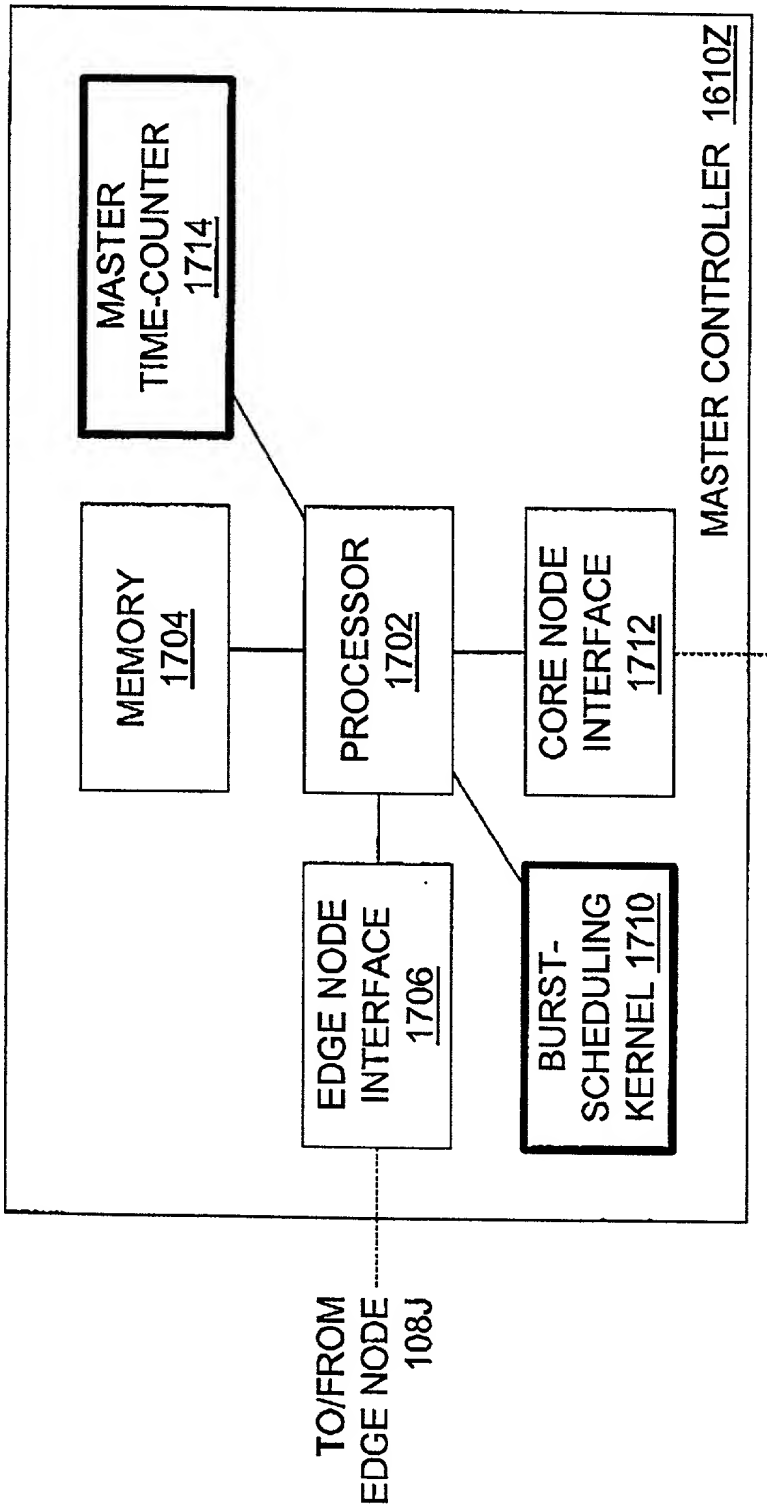
MASTER CONTROLLER 1610Z
MASTER TIME-COUNTER 1714
MEMORY 1704
PROCESSOR 1702
CORE NODE INTERFACE 1712
EDGE NODE INTERFACE 1706
BURST-SCHEDULING KERNEL 1710
TO/FROM EDGE NODE 108J
TO/FROM CORE NODE 110Z

FIG. 17

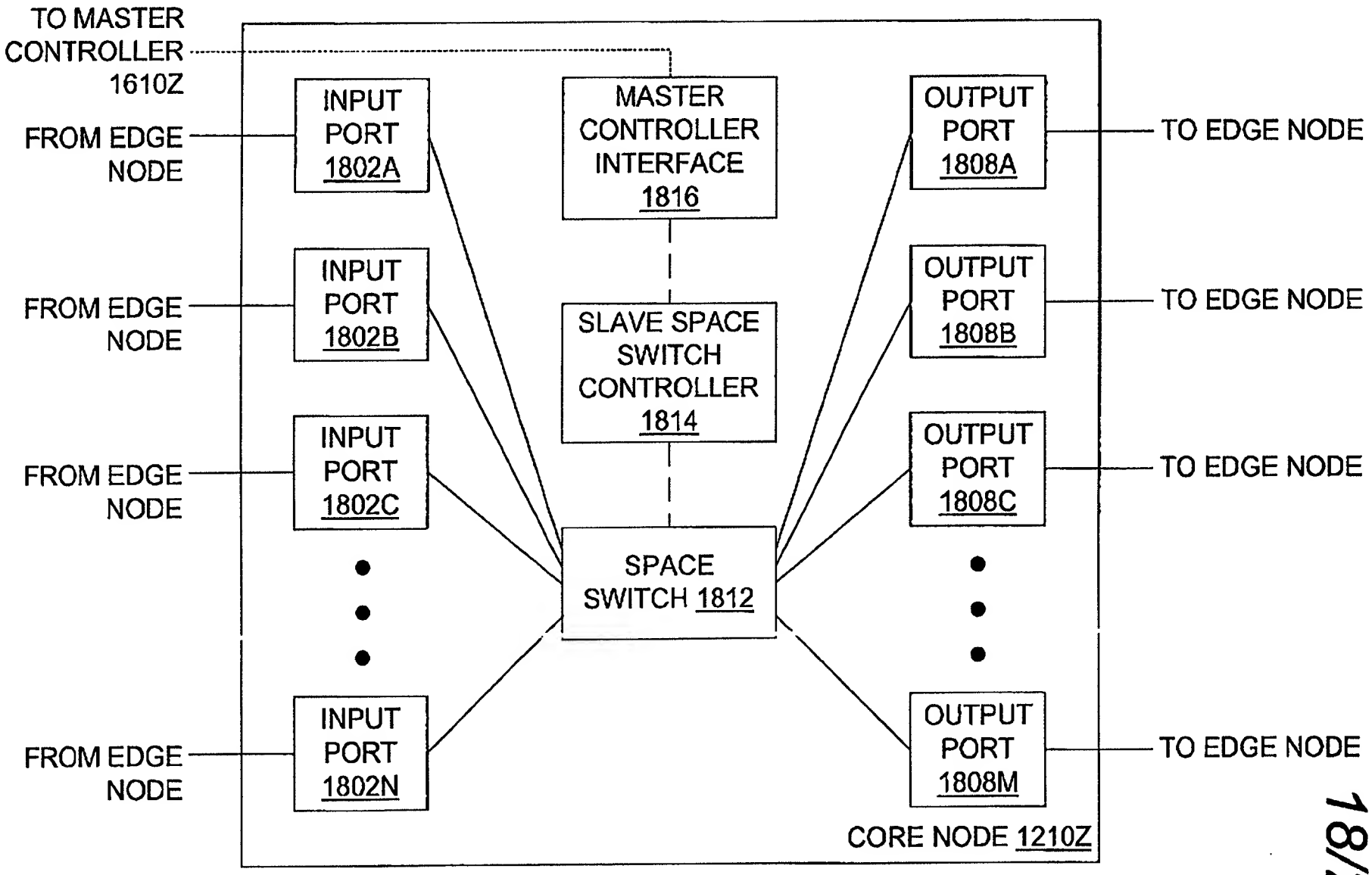


FIG. 18

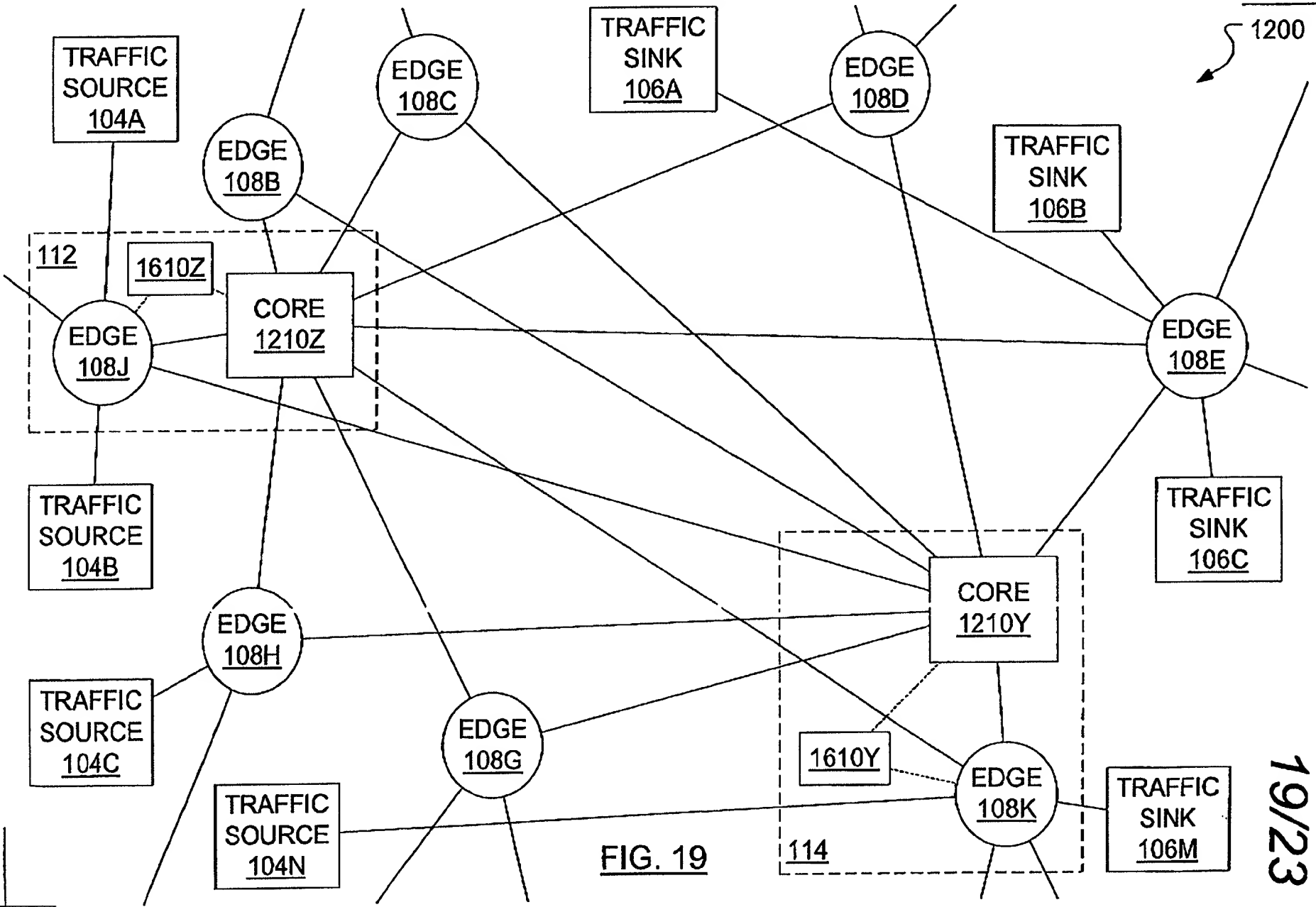


FIG. 19

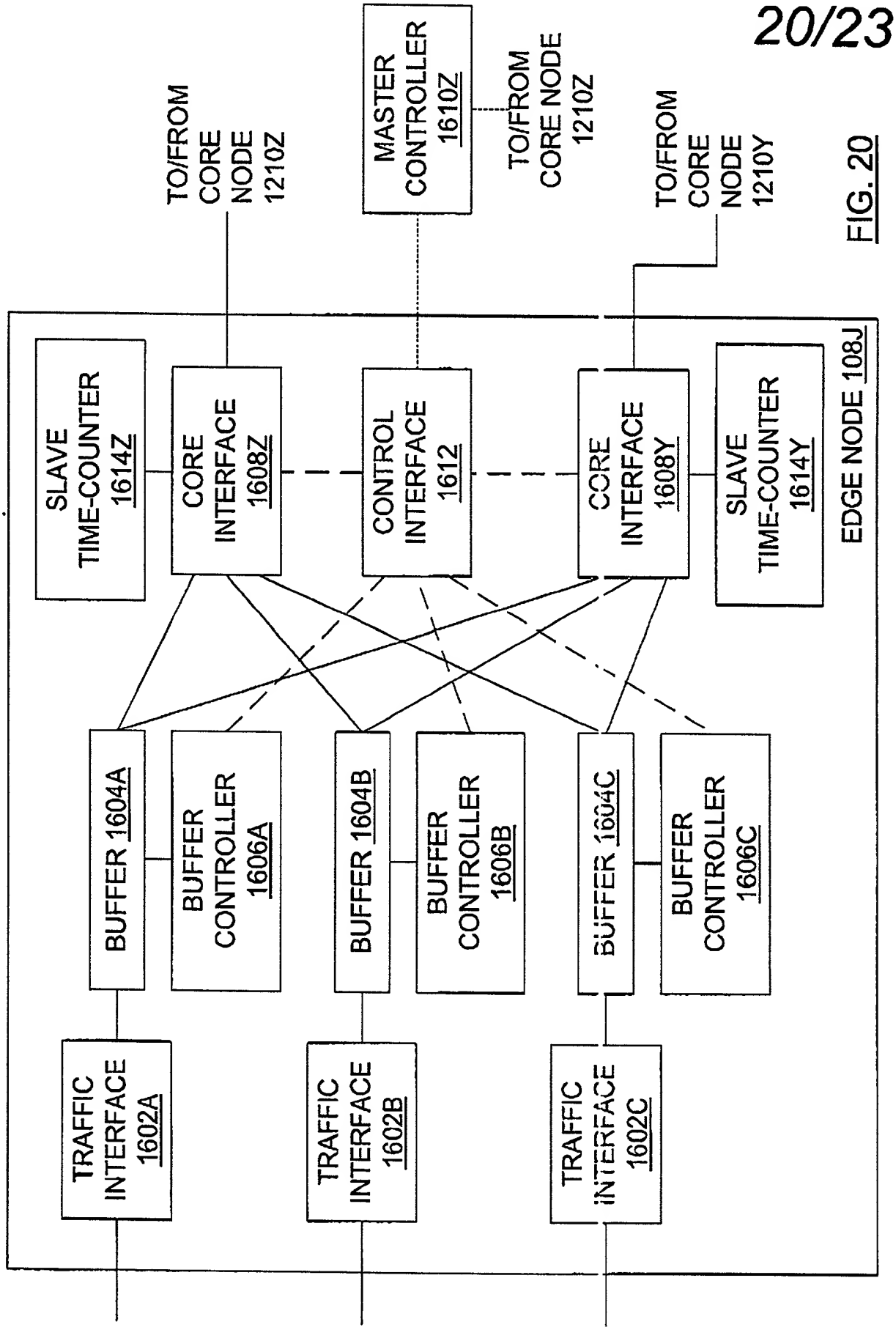
TO/FROM CORE NODE 1210Z
MASTER CONTROLLER 1610Z
TO/FROM CORE NODE 1210Z
TO/FROM CORE NODE 1210Y
SLAVE TIME-COUNTER 1614Z
CORE INTERFACE 1608Z
CONTROL INTERFACE 1612
CORE INTERFACE 1608Y
SLAVE TIME-COUNTER 1614Y
EDGE NODE 108J
BUFFER 1604A
BUFFER CONTROLLER 1606A
BUFFER 1604B
BUFFER CONTROLLER 1606B
BUFFER 1604C
BUFFER CONTROLLER 1606C
TRAFFIC INTERFACE 1602A
TRAFFIC INTERFACE 1602B
TRAFFIC INTERFACE 1602C

FIG. 20

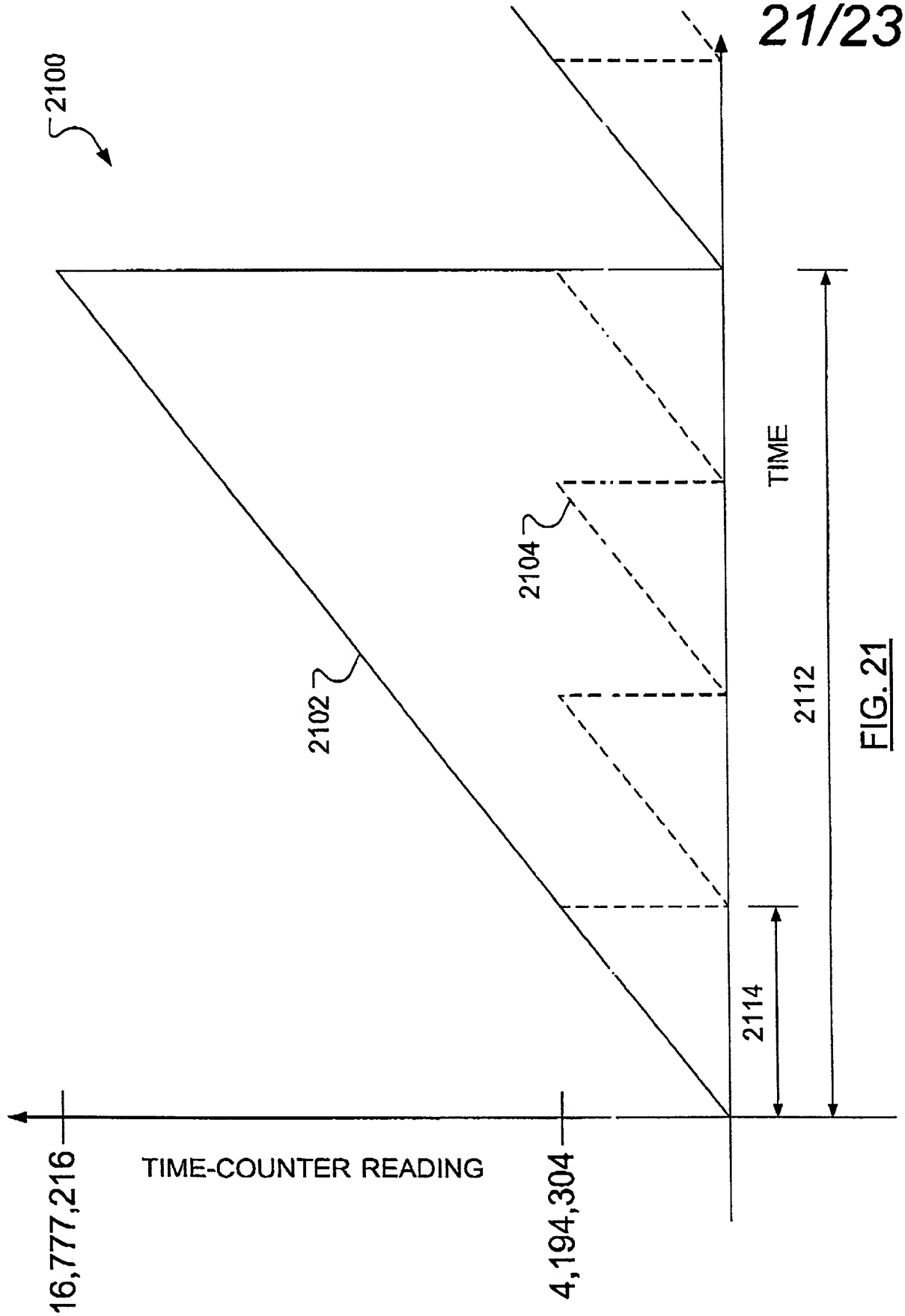
2100
2102
2104
TIME
2112
2114
16,777,216
TIME-COUNTER READING
4,194,304

FIG. 21

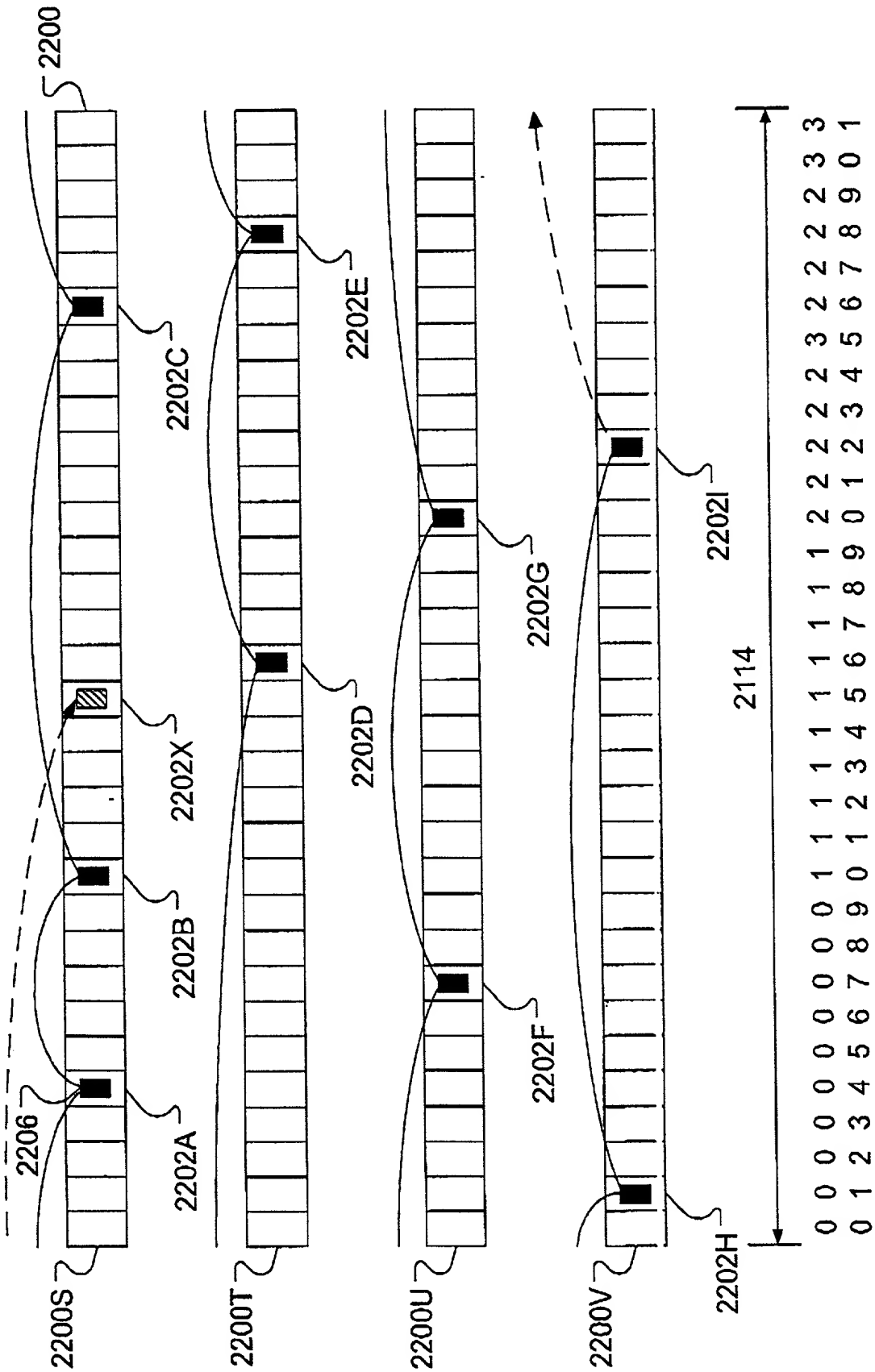
2200
2202C
2202E
2202X
2202B
2202D
2206
2202A
2202G
2202I
2202F
2114
2202H
2200S
2200T
2200U
2200V
0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 2 3 3
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1

FIG. 22

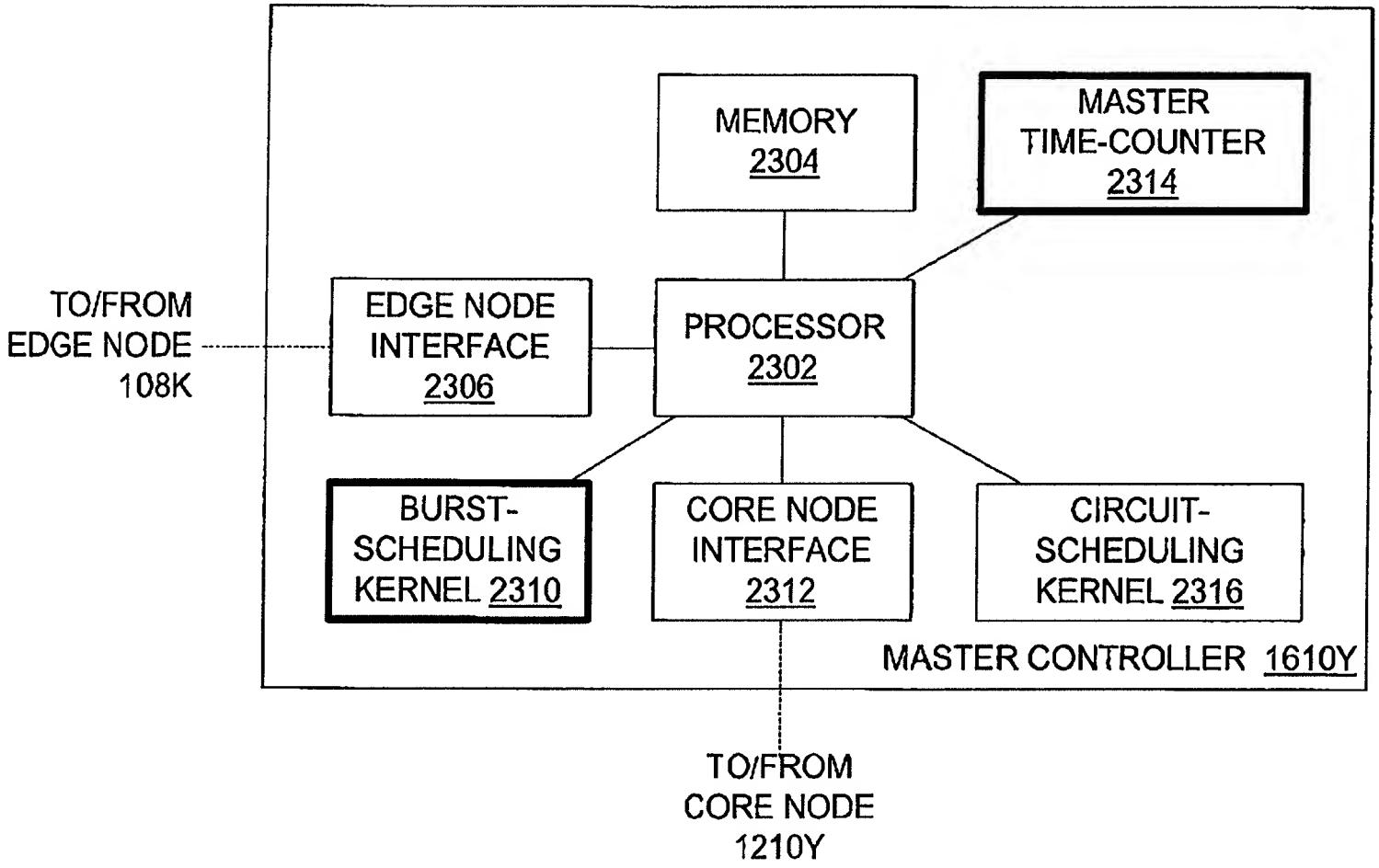


FIG. 23